**Laboratory # 14**

**OPEN- ENDED LAB**

**Simulate 4x1 Multiplexer**

**Objective:**

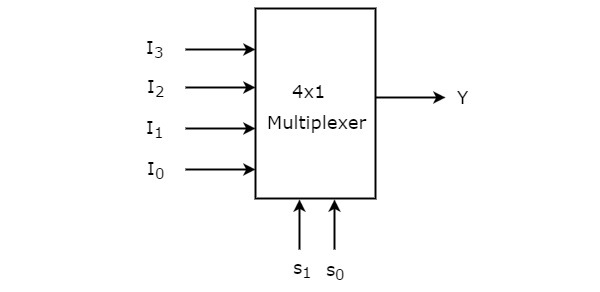
Trace and simulate a 4x1 multiplexer using Verilog.

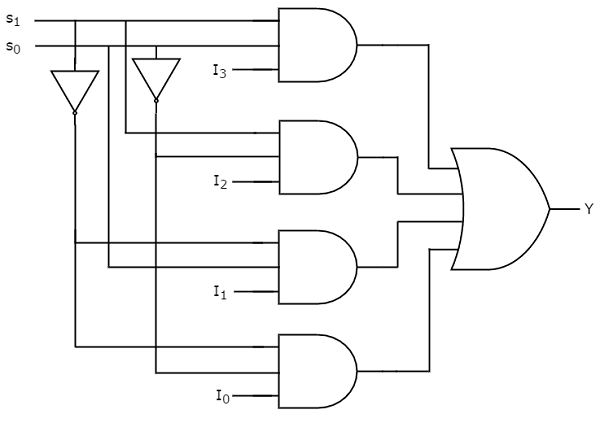
**Hardware/Software Required:**

IC 74153

Verilog

**Diagram:**





*4x1 Multiplexer Circuit Diagram*

|  |  |  |  |
| --- | --- | --- | --- |
| **Data Inputs** | **Select** | **Inputs** | **Outputs** |
| **D** | **S1** | **S0** | **Y** |
| D | 0 | 0 | I0 |
| D | 0 | 1 | I1 |
| D | 1 | 0 | I2 |
| D | 1 | 1 | I3 |

*Truth Table for 4x1 Multiplexer*

**Theory:**

A 4x1 multiplexer (MUX) is a digital circuit that selects one of the four input data lines and directs it to the single output line. The selection of the input line is controlled by a set of two selection lines, often called control lines or inputs. The term "4x1" indicates that there are four data inputs and one output.

**Steps to follow:**

**Step 1:**

* Write a code in Verilog module for 4x1 Multiplexer.

module mux4x1 (

input wire [3:0] data\_in, // 4-bit input data

input wire [1:0] sel, // 2-bit select line

output reg out // Output

);

always @(\*) begin

case (sel)

2'b00: out = data\_in[0];

2'b01: out = data\_in[1];

2'b10: out = data\_in[2];

2'b11: out = data\_in[3];

default: out = 1'b0; // Default value (optional)

endcase

end

endmodule

**Step 2:**

* Write a test bench code for 4x1 Multiplexer.

module mux4x1\_tb;

reg [3:0] data\_in;

reg [1:0] sel;

wire out;

mux4x1 uut (

.data\_in(data\_in),

.sel(sel),

.out(out)

);

initial begin

// Test case 1

data\_in = 4'b1100;

sel = 2'b00;

#10 $display("Output for test case 1: %b", out);

// Test case 2

data\_in = 4'b1100;

sel = 2'b01;

#10 $display("Output for test case 2: %b", out);

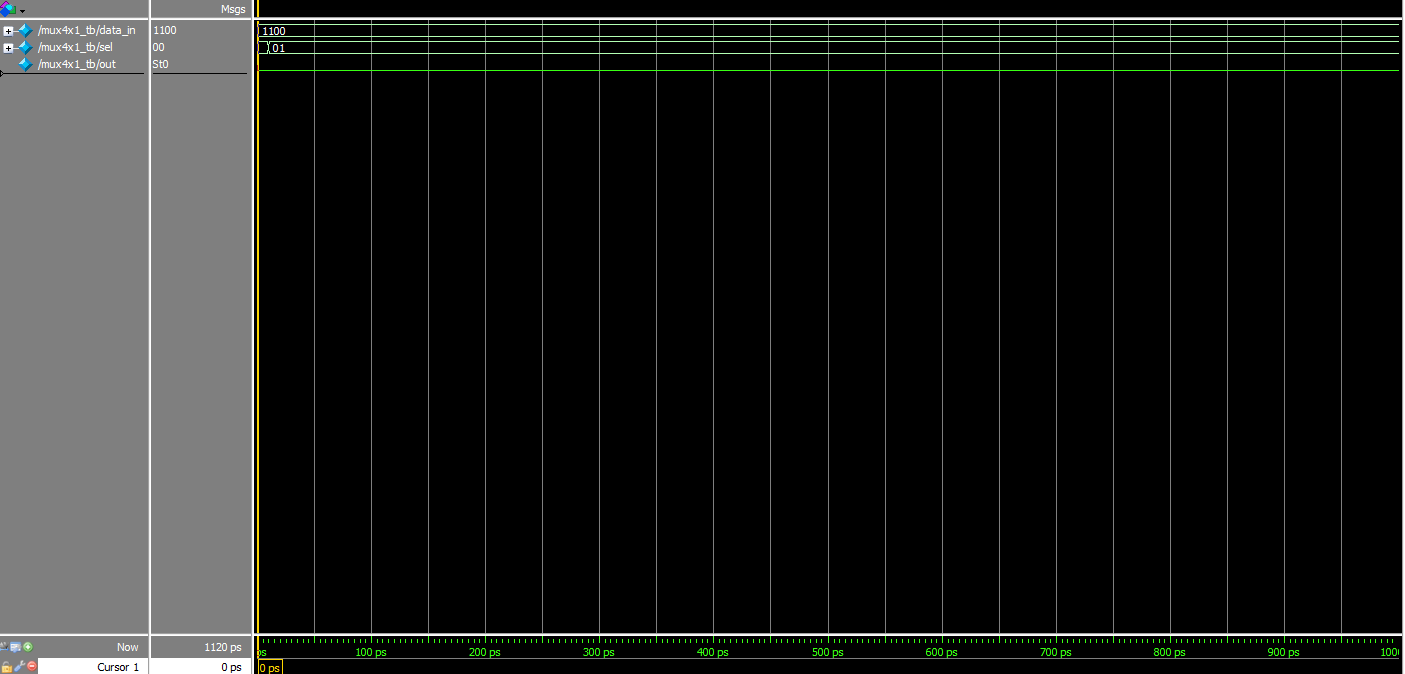
// Add more test cases as needed

$stop;

end

endmodule

**Observation:**

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**Conclusion:**

**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

Date: \_\_\_\_\_\_\_\_\_\_\_ Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_